19/715, 748

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Search Results -

Terms	Documents
l2 and (integration or integrating) and 438/$.ccls. and (distribute or distributing or diffuse or diffusing)	12

Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Refine Search: `l2 and (integration or integrating) and 438/$.ccls. and (distribute or distributing or diffuse or diffusing)` Clear

Search History

Today's Date: 4/21/2001

DB Name	Query	Hit Count	Set Name
USPT	l2 and (integration or integrating) and 438/$.ccls. and (distribute or distributing or diffuse or diffusing)	12	L5
USPT	l2 and (integration or integrating) and 438/$.ccls.	20	L4
USPT	l2 and (integration or integrating)	43	L3
USPT	l1 and conductivity and dielectric	150	L2
USPT	diode and (dopant or doping) and (cap or capping)and (implant or implanting) and mask	390	L1

Search run (p/n junction) w/s diode

& Cap layer & conductivity type

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Search Results - Record(s) 1 through 12 of 12 returned.

☐ 1. Document ID: US 6136652 A

L6: Entry 1 of 12 File: USPT Oct 24, 2000

US-PAT-NO: 6136652
DOCUMENT-IDENTIFIER: US 6136652 A
TITLE: Preventing dielectric thickening over a channel area of a split-gate transistor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw. Desc | Image

☐ 2. Document ID: US 5851864 A

L6: Entry 2 of 12 File: USPT Dec 22, 1998

US-PAT-NO: 5851864
DOCUMENT-IDENTIFIER: US 5851864 A
TITLE: Method of fabricating BiCMOS devices

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw. Desc | Image

☐ 3. Document ID: US 5744384 A

L6: Entry 3 of 12 File: USPT Apr 28, 1998

US-PAT-NO: 5744384
DOCUMENT-IDENTIFIER: US 5744384 A
TITLE: Semiconductor structures which incorporate thin film transistors

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw. Desc | Image

☐ 4. Document ID: US 5643820 A

L6: Entry 4 of 12 File: USPT Jul 1, 1997

US-PAT-NO: 5643820
DOCUMENT-IDENTIFIER: US 5643820 A
TITLE: Method for fabricating an MOS capacitor using zener diode region

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 5. Document ID: US 5393681 A

L6: Entry 5 of 12 File: USPT Feb 28, 1995

US-PAT-NO: 5393681
DOCUMENT-IDENTIFIER: US 5393681 A
TITLE: Method for forming a compact transistor structure

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 6. Document ID: US 5342794 A

L6: Entry 6 of 12 File: USPT Aug 30, 1994

US-PAT-NO: 5342794
DOCUMENT-IDENTIFIER: US 5342794 A
TITLE: Method for forming laterally graded deposit-type emitter for bipolar transistor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 7. Document ID: US 5283202 A

L6: Entry 7 of 12 File: USPT Feb 1, 1994

US-PAT-NO: 5283202
DOCUMENT-IDENTIFIER: US 5283202 A
TITLE: IGBT device with platinum lifetime control having gradient or profile tailored platinum diffusion regions

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 8. Document ID: US 5262336 A

L6: Entry 8 of 12 File: USPT Nov 16, 1993

US-PAT-NO: 5262336
DOCUMENT-IDENTIFIER: US 5262336 A
TITLE: IGBT process to produce platinum lifetime control

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 9. Document ID: US 5223449 A

L6: Entry 9 of 12 File: USPT Jun 29, 1993

US-PAT-NO: 5223449
DOCUMENT-IDENTIFIER: US 5223449 A
TITLE: Method of making an integrated circuit composed of group III-V compound field effect and bipolar semiconductors

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 10. Document ID: US 5075241 A

L6: Entry 10 of 12 File: USPT Dec 24, 1991

US-PAT-NO: 5075241
DOCUMENT-IDENTIFIER: US 5075241 A
TITLE: Method of forming a recessed contact bipolar transistor and field effect device

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 11. Document ID: US 4985744 A

L6: Entry 11 of 12 File: USPT Jan 15, 1991

US-PAT-NO: 4985744
DOCUMENT-IDENTIFIER: US 4985744 A
TITLE: Method for forming a recessed contact bipolar transistor and field effect transistor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 12. Document ID: US 4849344 A

L6: Entry 12 of 12 File: USPT Jul 18, 1989

US-PAT-NO: 4849344
DOCUMENT-IDENTIFIER: US 4849344 A
TITLE: Enhanced density modified isoplanar process

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Terms	Documents
15	12

Display 12 Documents, starting with Document: 12

Display Format: TI Change Format